FAST VCO CALIBRATION FOR FREQUENCY SYNTHESIZERS

BACKGROUND OF THE INVENTION

Field of the Invention:

This invention relates to frequency synthesizers, particularly to the voltage-controlled oscillator (VCO) of a frequency synthesizers for radio transceivers.

Brief Description of Related Art

In wireless communications system, frequency synthesizers are used to generate stable local oscillator (LO) frequencies with very high accuracy. A frequency synthesizer is usually a phase-locked loop (PLL) whose simplified diagram is shown in Figure 1 It consists of a reference frequency divider (1/M), a feedback frequency divider (1/N), a phase comparator (PC), a charge pump (CP), a loop filter (LPF) and a VCO. Under phase-locked condition, the frequencies of the two signals at the PC inputs are identical. This forces the VCO frequency (Fout) to be N/M of the input reference frequency (Fref).

Usually the center frequency of a free-running VCO exhibits large variations over process and temperature. In order to generate the desired LO frequency, the frequency tuning range of the VCO needs to be large enough to overcome the above variations. Unfortunately, this leads to a large VCO gain (Kvco), which results in poor phase noise of the PLL.

To increase the tuning range of the VCO without sacrificing the phase noise performance, Welland proposed in U.S. Pat. No. 6,137,372 to use a coarse tuning arrangement in conjunction with fine tuning for the VCO. The VCO is designed in such a way that its frequency can be controlled both discretely through some digital bits and continuously through an analog voltage. The digital control varies the VCO frequency over a large range with coarse steps; while the analog control tunes the VCO frequency over a much narrower range.

Chien proposed in U.S. Pat. No. 6,597,249 a binary search algorithm to find the optimal digital control word. The binary search algorithm greatly reduces the search time compared to a linear search algorithm.

SUMMARY OF THE INVENTION

An object of this invention is to minimize the VCO gain without scarifying the tolerance of process and temperature variation of the VCO. Another object of the invention is to improve the

phase noise performance of the PLL. Still another of this invention is to shorten the settling time of a frequency synthesizer.

These objects are achieved by first calibrating the VCO to within a small tolerance of the desired VCO control voltage. The VCO frequency is incremented or decremented according the to frequency measurement result. When the VCO frequency error is large during calibration, the control word is changed in discrete steps to bring the frequency of the VCO to within a preset tolerance. When the VCO frequency is close to the desired frequency, the PLL is switched to a conventional analog operating mode to accurately lock the VCO frequency with the reference frequency. This results in a shorter search time than prior art, and allows calibration during channel switching. This not only achieves more accurate results than prior art, but also potentially supports frequency hopping in the RF wireless communications. It also eliminates the need for a look-up table to store the calibration results for all the RF channels, which results in a more efficient hardware implementation.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 shows a block diagram of a phase-locked loop (PLL)

Fig.2 shows a calibration circuit for a PLL based on the present invention.

Fig. 3 shows the frequency of the VCO as function of different control voltage steps.

Fig. 4 shows the feedback divider output frequency vs control voltage steps.

Fig.5 shows a block diagram of the VCO calibration circuit.

Fig.6 shows the state transition diagram of the counter block in the calibration circuit.

Fig.7 shows the state transition diagram of the decision making block in the calibration block

Fig.8 shows the simulation result of the VCO control voltage steps.

Fig. 9 shows the calibration errors of the VCO control voltage steps.

Fig.10 shows the required time for calibration.

Table 1 shows the pin description.

DETAILED DESCRIPTION OF THE INVENTION

The synthesizer of the present invention operates with two sequential modes; a calibration mode and an analog mode. During the calibration mode, the synthesizer locks the frequency of a VCO coarsely but rapidly to the reference frequency using a first phase-locked loop by generating an

approximate control voltage for the VCO and to set the VCO frequency within a certain tolerance. This approximate control voltage is used to start operating a conventional phase-locked loop in the analog mode for fine tuning of the VCO.

The calibration circuit with the PLL is drawn in Figure 2. The calibration PLL uses a FS_CAL block as a coarse phase detector instead of the conventional PC+CP phase detector shown in Fig.1. The calibration is triggered by a rising edge of fsCalStart to FS_CAL. It first breaks the conventional PLL loop by raising EN signal to enable FS_CAL. Now the VCO control input is connected to a fixed reference voltage vcoStep[4.0] derived and held from the FS_CAL phase detector. The frequency of the free-running VCO is divided down to a frequency close to 1MHz and fed back to the FS_CAL phase detector through vcoDiv lead, and its period is measured with a 44MHz clock. After calibration is finished, EN is reset to 0, and the analog PLL loop including a phase comparator and a charge pump phase detector is closed or enabled.

The nominal VCO frequency at room temperature is shown in Figure 3 as a function of its analog control voltage for each stepped value of vcoStep[4:0]. It varies over process and temperature. The VCO output frequency is divided by 2N and measured at the feedback divider in the PLL. Fig.4 shows the feedback divider output frequency as a function of vcoStep value for a given control voltage of the VCO. The curve also varies over process and temperature. By setting the correct value of vcoStep[4:0], the divider output frequency is trimmed closest to 1MHz, which is the target frequency for phase locking. For a fixed control voltage, the frequency resolution at the divider output is about 6.122kHz for a single LSB step of vcoStep.

A block diagram of the calibration circuit is shown in Figure 5. It includes a 10-bit counter CNT and a decision making block DCSN. The I/O pins are described in Table I. CNT counts the clock CLK, and indicates whether to increment or to decrement vcoStep of DCSN, which is a control unit that enables or disables CNT through EN, and calculates the VCO control value vcoStep[4:0]. EN signal also breaks or reconnects the PLL loop.

The counter CNT and the decision making block DCSN are finite state machines whose state transition diagrams are shown in Figure 6 and Figure 7. At the end of the calibration, the calibration result should be held at vcoStep[4:0], and the signal Rdy2Cal should be held high, indicating the finish of the calibration. The circuit should be able to start again at the next rising edge of the signal fsStart. vcoErr is set low if the calibration was successful. Otherwise, vcoErr is set high indicating an error is VCO calibration.

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The counter CNT is powered up when EN is high. First it waits for about 23us by counting 1023 clock cycles. This allows enough time for the VCO control to settle to the reference voltage Vref. Then it starts to count for every cycle of vcoDiv, which is the feedback divider output. If the period of vcoDiv is less then 43 clock cycles, it means that the VCO is too fast. Therefore, it sets U/D to -1, indicating a decrement of vcoStep. If the period of vcoDiv is more than 45 clock cycles, it means that the VCO is too slow. Therefore, it sets U/D to +1, indicating an increment of vcoStep. If the measurement is between 43 and 45, it implies that the VCO frequency is close to the target. It will set U/D to 0, indicating no change of vcoStep, and keep counting into the next vcoDiv cycle without resetting its value.

The decision making block DCSN is triggered by the rising edge of fsStart. Then it sets EN to high, which activates the counter CNT, breaks the PLL loop, and sets the VCO control voltage to Vref. It updates vcoStep based on the signal U/D. This pulls the VCO frequency close to the target frequency. When it sees vcoStep remain unchanged for 8 consecutive times or vcoStep start to head into a different direction, it enters averaging mode. It takes the average of 16 consecutive values of vcoStep, and take it as the final calibration result. During any of the above steps, if vcoStep overflows or underflows by trying to reach 32 or -1, vcoErr is raised high to indicate an error in the calibration process. However, the calibration continues normally with vcoStep clipped at 31 or 0.

The calibration algorithm described above has been implemented in a C++ program. The VCO center frequency is swept, and the calibrated vcoStep is shown in Fig.8. VCO phase noise of -100dBc/Hz at 1MHz offset from 2.45GHz is assumed. The calibrated vcoStep result is compared with the ideal result. Figure 9 plots the calibration error, which is confined within $\pm$0.7LSB. Figure 10 shows the required time for the VCO calibration according to our simulation. The maximum time required is about 110us.

We have invented a VCO calibration algorithm, which trims the VCO center frequency to the desired value. The circuit works with a 44MHz clock. The total time required for the calibration is less than 110us. Rdy2Cal is raised to indicate the finish of calibration. vcoErr is raised to indicate an error.

While the preferred embodiment of the invention has been described, it will be apparent to those skilled in the art that various modifications may be made in the embodiment without departing from the spirit of the present invention. Such modifications are all within the scope of this invention.

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